S/N Unknown PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Gary R. Gilliam	Examiner: Unknown
Serial No.:	Unknown	Group Art Unit: Unknown
Filed:	Herewith	Docket: 303.221US3
Title:	ON-CHIP SUBSTRATE REGULATOR TEST MODE	

PRELIMINARY AMENDMENT

BOX PATENT APPLICATON
Commissioner for Patents
Washington, D.C. 20231

Sir:

When the above-identified patent application is taken up for consideration, please amend the application as follows:

IN THE SPECIFICATION

On page 1, line 3, before the heading "Field of the Invention," insert the following paragraph:

Cross Reference to Related Application(s)

This application is a division of U.S. Application No. 09/065,139, filed on April 23, 1998, which is a division of U.S. Application No. 08/520,818, filed on August 30, 1995, now issued as U.S. Patent No. 5,880,593, the specifications of which are hereby incorporated by reference.

Please substitute the following paragraphs of the Specification with the paragraphs in the appendix entitled "Clean Version of Specification Paragraphs." Following are marked-up versions of the amended paragraphs showing specific changes:

The paragraph beginning on page 4, line 19, is amended as follows:

For example, in Figure 1, the non-test condition of EN1 may be at a logical [los] low so that the MOSFET M3 is in the diode chain because the MOSFET M4 is off. The non-test condition of EN2 may be at a logical high so that the MOSFET M5 is essentially shorted out of the diode chain because the MOSFET M6 is on. Therefore, the voltage level of the substrate at node Vbb, under non-test conditions, is substantially equivalent to the supply voltage level Vcc, less the voltage dropped by the three MOSFETs M1, M2 and M3. Under test conditions, the

voltage level at node Vbb can be made more positive by raising the control signal EN1 to a logical high. Such an enabling of the control signal EN1 turns on the MOSFET M4 which essentially shorts the channel of the MOSFET M3 thereby removing the MOSFET M3 from the diode chain, so that the voltage level at Vbb is substantially equivalent to the supply voltage level Vcc, less the voltage dropped by only the MOSFETs M1 and M2. The normal substrate voltage level at Vbb can then be restored by returning the control voltage EN1 to a logical low.

The paragraph beginning on page 6, line 16, is amended as follows:

The addition of the MOSFETs M7, M8, M9 and M10 to the circuit increases the adjustability of the substrate voltage level Vbb, beyond that of the circuit shown in Figure 1. For example, the non-test condition for the control signals EN1 and EN2 may be a logical [los] <u>low</u> so that the MOSFETs M3 and M5 are in the diode chain. The non-test condition for the control signals EN3 and EN4 may be a logical high so that the MOSFETs M7 and M8 are essentially shorted out of the diode chain. Under test conditions, the substrate voltage level Vbb may be made more positive by raising the control signal EN1 to a logical high and essentially shorting the MOSFET M3 out of the diode chain. The substrate voltage level Vbb can then be made even more positive by raising the control signal EN2 to a logical high and essentially shorting the MOSFET M5 out of the diode chain, as well. The normal substrate voltage level at Vbb can then be restored by returning the control signals EN1 And EN2 to a logical low. The substrate voltage level Vbb, can be made more negative from its non-test condition by lowering the control signal EN3 to a logical low and thereby adding the MOSFET M7 to the diode chain. The substrate voltage level Vbb, can then be made even more negative by lowering the control signal EN4 to a logical low and adding the MOSFET M9 to the diode chain.

IN THE CLAIMS

Please cancel claims 1-18 after adding the following new claims:

19. A method of testing an integrated circuit by adjusting a semiconductor substrate bias voltage, the method comprising the steps of:

coupling the semiconductor substrate to a positive voltage supply through a series of resistive elements such that a voltage drop through the resistive elements defines a semiconductor substrate bias voltage having a first negative voltage level;

reducing the semiconductor substrate bias voltage to a second negative voltage level which is lower than the first negative voltage level by increasing the voltage drop through the resistive elements; and

increasing the semiconductor substrate bias voltage to a third negative voltage level which is higher than the first negative voltage level by decreasing the voltage drop through the resistive elements.

20. The method of claim 19 wherein the series of resistive elements are diodes.

21. The method of claim 20 wherein the step of reducing the semiconductor substrate bias comprises the step of electrically adding at least one additional diode to the series of diodes by deactivating a bypass transistor.

22. The method of claim 20 wherein the step of increasing the semiconductor substrate bias comprises the step of electrically removing at least one additional diode from the series of diodes by activating a bypass transistor.

23. (New) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diodes between a supply voltage source and the

substrate; and

coupling at least one bypass transistor to at least one diode in the series of diodes for electrically bypassing at least one diode.

24. (New) The method of claim 23 wherein coupling at least one bypass transistor to at least one diode includes coupling a plurality of bypass transistors to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

25. (New) The method of claim 23 wherein coupling at least one bypass transistor to at least one diode includes coupling at least one bypass transistor to plurality of diodes for electrically bypassing the plurality of diodes.

26. (New) The method of claim 23 wherein coupling at least one bypass transistor to at least one diode includes coupling at least one normally off bypass transistor to at least one diode leaving the at least one diode unbypassed during normal operation and allowing the at least one diode to be selectively bypassed during testing operations.

27. (New) The method of claim 23 wherein coupling at least one bypass transistor to at least one diode includes coupling at least one normally on bypass transistor to at least one diode leaving the at least one diode bypassed during normal operation and allowing the at least one diode to be selectively unbypassed during testing operations.

28. (New) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diodes between a supply voltage source and the substrate; and

coupling at least one bypass transistor to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

29. (New) The method of claim 28 wherein coupling at least one bypass transistor to a plurality of diodes includes coupling at least one normally off bypass transistor to a plurality of diodes leaving the plurality of diodes unbypassed during normal operation and allowing the plurality of diodes to be selectively bypassed during testing operations.

30. (New) The method of claim 28 wherein coupling at least one bypass transistor to a plurality of diodes includes coupling at least one normally on bypass transistor to a plurality of diodes leaving the plurality of diodes bypassed during normal operation and allowing the plurality of diodes to be selectively unbypassed during testing operations.

31 (New) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diodes between a supply voltage source and the substrate; and

coupling a plurality of bypass transistors to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

32. (New) The method of claim 31 wherein coupling a plurality of bypass transistors to a plurality of diodes includes coupling a plurality of normally off bypass transistors to a plurality of diodes leaving the plurality of diodes unbypassed during normal operation and allowing the plurality of diodes to be selectively bypassed during testing operations.

33. (New) The method of claim 31 wherein coupling a plurality of bypass transistors to a plurality of diodes includes coupling a plurality of normally on bypass transistors to a plurality of diodes leaving the plurality of diodes bypassed during normal operation and allowing the plurality of diodes to be selectively unbypassed during testing operations.

34. (New) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diode connected transistors between a supply voltage source and the substrate; and

coupling at least one bypass transistor to at least one diode connected transistor in the series of diode connected transistors for electrically bypassing at least one diode connected transistor.

35. (New) The method of claim 34 wherein coupling at least one bypass transistor to at least one diode connected transistor includes coupling at least one bypass transistor to plurality of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

36. (New) The method of claim 34 wherein coupling at least one bypass transistor to at least one diode connected transistor includes coupling at least one normally off bypass transistor to at least one diode connected transistor leaving the at least one diode connected transistor unbypassed during normal operation and allowing the at least one diode connected transistor to be selectively bypassed during testing operations.

37. (New) The method of claim 34 wherein coupling at least one bypass transistor to at least one diode connected transistor includes coupling at least one normally on bypass transistor to at least one diode connected transistor leaving the at least one diode connected transistor bypassed during normal operation and allowing the at least one diode connected transistor to be selectively unbypassed during testing operations.

38. (New) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diode connected transistors between a supply voltage source and the substrate; and

coupling at least one bypass transistor to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

39. (New) The method of claim 38 wherein coupling at least one bypass transistor to a plurality of diode connected transistors includes coupling a plurality of bypass transistors to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

40. (New) The method of claim 38 wherein coupling a plurality of bypass transistors to a plurality of diode connected transistors includes coupling a plurality of normally off bypass transistors to a plurality of diode connected transistors leaving the plurality of diode connected transistors unbypassed during normal operation and allowing the plurality of diode connected transistors to be selectively bypassed during testing operations.

41. (New) The method of claim 38 wherein coupling a plurality of bypass transistors to a plurality of diode connected transistors includes coupling a plurality of normally on bypass transistors to a plurality of diode connected transistors leaving the plurality of diode connected transistors bypassed during normal operation and allowing the plurality of diode connected transistors to be selectively unbypassed during testing operations.

42. (New) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diode connected transistors between a supply voltage source and the substrate; and

coupling a plurality of bypass transistors to a plurality of diode connected

transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

43. (New) The method of claim 42 wherein coupling a plurality of bypass transistors to a plurality of diode connected transistors includes coupling a plurality of normally off bypass transistors to a plurality of diode connected transistors leaving the plurality of diode connected transistors unbypassed during normal operation and allowing the plurality of diode connected transistors to be selectively bypassed during testing operations.

44. (New) The method of claim 42 wherein coupling a plurality of bypass transistors to a plurality of diode connected transistors includes coupling a plurality of normally on bypass transistors to a plurality of diode connected transistors leaving the plurality of diode connected transistors bypassed during normal operation and allowing the plurality of diode connected transistors to be selectively unbypassed during testing operations.

REMARKS

Claims 1 - 18 have been canceled and new claims 19 - 44 have been added. Claims 19 - 44 are now pending in this application.

The specification is amended to add a cross reference to the prior application. No new matter is added by way of these amendments.

The application filing fee as calculated on the application transmittal sheet reflects the amendments to the claims described above.

The Applicant respectfully requests that the preliminary amendment described herein be entered into the record prior to examination and consideration of the above-identified application.

Respectfully submitted,

GARY R. GILLIAM

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This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

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WD #

Clean Version of the Amended Specification Paragraphs

ON-CHIP SUBSTRATE REGULATOR TEST MODE
Applicant: Gary R. Gilliam
Serial No.: Unknown

Please replace the paragraph beginning on page 4, line 19, with the following:

For example, in Figure 1, the non-test condition of EN1 may be at a logical low so that the MOSFET M3 is in the diode chain because the MOSFET M4 is off. The non-test condition of EN2 may be at a logical high so that the MOSFET M5 is essentially shorted out of the diode chain because the MOSFET M6 is on. Therefore, the voltage level of the substrate at node Vbb, under non-test conditions, is substantially equivalent to the supply voltage level Vcc, less the voltage dropped by the three MOSFETs M1, M2 and M3. Under test conditions, the voltage level at node Vbb can be made more positive by raising the control signal EN1 to a logical high. Such an enabling of the control signal EN1 turns on the MOSFET M4 which essentially shorts the channel of the MOSFET M3 thereby removing the MOSFET M3 from the diode chain, so that the voltage level at Vbb is substantially equivalent to the supply voltage level Vcc, less the voltage dropped by only the MOSFETs M1 and M2. The normal substrate voltage level at Vbb can then be restored by returning the control voltage EN1 to a logical low.

Please replace the paragraph beginning on page 6, line 16, with the following:

The addition of the MOSFETs M7, M8, M9 and M10 to the circuit increases the adjustability of the substrate voltage level Vbb, beyond that of the circuit shown in Figure 1. For example, the non-test condition for the control signals EN1 and EN2 may be a logical low so that the MOSFETs M3 and M5 are in the diode chain. The non-test condition for the control signals EN3 and EN4 may be a logical high so that the MOSFETs M7 and M8 are essentially shorted out of the diode chain. Under test conditions, the substrate voltage level Vbb may be made more positive by raising the control signal EN1 to a logical high and essentially shorting the MOSFET M3 out of the diode chain. The substrate voltage level Vbb can then be made even more positive

by raising the control signal EN2 to a logical high and essentially shorting the MOSFET M5 out of the diode chain, as well. The normal substrate voltage level at Vbb can then be restored by returning the control signals EN1 And EN2 to a logical low. The substrate voltage level Vbb, can be made more negative from its non-test condition by lowering the control signal EN3 to a logical low and thereby adding the MOSFET M7 to the diode chain. The substrate voltage level Vbb, can then be made even more negative by lowering the control signal EN4 to a logical low and adding the MOSFET M9 to the diode chain.